SPECIAL REPORT

for

THE EFFECTS OF SPACE RADIATION ON SILICON INTEGRATED MICROCIRCUITS (U)

29 June - 31 December 1965

Contract No. NAS5-9630

Prepared by

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for

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SUMMARY

The object of this report is to provide a description of the first 6 months of work under this program. During the period, as anticipated in the work statement, most of the devices to be studied have been obtained, measurement circuitry has been developed, preirradiation characterization has been started and is nearing completion, and measurement procedures and circuitry, and equipment for the actual irradiation have been and are being modified.

No conclusions are as yet warranted by these extensive but preliminary efforts. It is recommended that state-of-the-art-type devices for future programs be purchased and not obtained gratis.

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THE EFFECTS OF SPACE RADIATION ON SILICON INTEGRATED MICROCIRCUITS (U)

INTRODUCTION

This report covers the first 6 months of the program (June 29 through December 31, 1965), and describes the work accomplished during this period. The objective of the program is to classify four categories of integrated circuits according to their electron-radiation susceptibility.

The program is divided into six consecutive parts: (1) analysis of the microcircuits to determine measurements to be made and the measurement procedures to be used; (2) complete preirradiation, electrical characterization of the devices; (3) instrumentation modifications; (4) electrical monitoring during and measurements, related to the actual irradiation, such as dosimetry and temperature; (5) postirradiation characterization, as complete as electrical operations will allow; and (6) analysis of results.

The work described in this report is that of the partial completion of the first three parts of the program. Under these three parts, most of the devices have been obtained and analyzed, and the measurement procedures and most of the preirradiation characterization completed. The instrumentation modifications are, however, slightly less than half completed.

Devices to be Studied

The devices chosen for study in this program are digital and linear silicon integrated microcircuits. The devices consist of gates, flip-flops, and amplifiers chosen from several manufacturers and representing various categories of device types. Table 1 summarizes the choices under the preceding criteria. The letter-number in the table represents the manufacturer part-designation coding as previously furnished to Mr. F. Gordon by letter on September 20, 1965.

TABLE 1. MICROCIRCUITS CHOSEN FOR STUDY

Category of Device \ Type of Device	Gates	Flip-Flops	Amplifiers
Dielectric Isolation	B-3 G-1		
MOS	K-1 A-8	K-2	
Micropower	I-1	I-2 J-4	
Operational			A-7 H-1
Differential			C-3

Characterization

Preirradiation electrical characterization of the devices required analysis of them in order to determine what measurements should be made and the methods of making them. The work on the previous contract, NAS5-3985, was reviewed to indicate areas that could be improved or eliminated. Several of the more noticeable changes that resulted are the deletion of the capacitance-voltage measurements and the lifetime measurements, with emphasis on obtaining more and better gain and V_{SAT} measurements. A majority of this work has been completed, and the degree of completion is summarized in Table 2. It should

be noted here that the I-2 devices have not yet been delivered. Their second revised delivery date is January 17, 1966.

TABLE 2. CHARACTERIZATION COMPLETED DURING REPORT PERIOD

Manufacturer-Part Code	Device Number 1-5	6-10	11-15
A-7	C[a]	C	C
A-8	C	C	C
B-3	C	C	C
C-3	O[b]	O	O
G-1	4/8[c]	4/8	4/8
H-1	C	C	C
I-1	C	C	C
I-2	(d)	(d)	(d)
J-4	(e)	(e)	(e)
K-1	C	C	C
K-2	C	C	C

(a) C = Tests completed.

(b) O means devices on hand, but no characterization done.

(c) 4/8 = 4 of 8 tests completed.

(d) Not yet received from manufacturers.

(e) Nine samples have been characterized, six samples were out of specification and were returned to manufacturer for replacement.

Appendix I gives in detail the measurements made on amplifier Type H-1. This example includes the schematics for both the measurement circuits and the measurement procedures used. Examples of plans for the other device types were not included, since they are very similar to the example plan, or the plans used on the previous project NAS5-3985. A complete volume of the procedural information for all device types will be presented in the final report.

Instrumentation

Modifications in the instrumentation for irradiation have been partially completed. The Faraday cup and the counter circuit were completely rebuilt. The cup was enlarged and better insulating material used. The counter circuit had been exposed to the radiation during the previous program and it was felt that accuracy and precision could be increased by rebuilding it. It has been decided to load the dynamic devices for worst case so that they will be compatible with the statically operated devices. This loading may swamp out any changes that would occur in frequency of operation of these devices. However, measurements with fan-outs of one could be taken before and after irradiation, to obtain indications of any total change that has occurred. It also has been decided to modify the irradiation-test jig in order to better control the temperature of the devices, and to ease the handling of different device types. The work on the test jig is yet to be performed.

New Technology

No information or developments apply to this section.

Future Plans

The next reporting period under this program will include the completion of the preliminary characterization as described above and in Appendix I, the performance of the irradiation, the postirradiation characterization and analysis of results, and the preparation of the Final Report. The irradiation part of the program currently will consist of the irradiation of 10 devices of each device type in a 3 Mev electron environment. Five of each type will be in a dynamic operating configuration, and the other five will be in a static configuration. These devices will be monitored during the irradiation. The monitoring procedures will be similar to the ones that were used on the previous program. Five other devices of each type will be retained as controls.

It is expected that the five additional devices of each type will be irradiated in a nonenergized condition under an expansion of the current contract. These devices however, will be periodically checked by the use of pulsed measurements ($\sim$ 1 μsec) and also checked after exposure by observing them in a configuration similar to those in the static operating condition. A proposal has been submitted for this expansion and should be acted upon during January, 1966.

The electron radiation will be provided by a 3.0 Mev Van de Graaff generator, and the total exposure will be sufficient to cause significant degradation of the microcircuits (10^{15} - 10^{16} electrons/cm^2, or more as required.

The postirradiation characterization will be essentially the same as that described for the preirradiation measurements. Some modifications may be necessary because of the radiation-induced changes in the microcircuits.

The data analysis will be performed to determine the type and degree of effects due to radiation, to compare the relative behavior of the various classes of circuits studied, and, where so indicated, to recommend changes that would provide increased radiation tolerance.

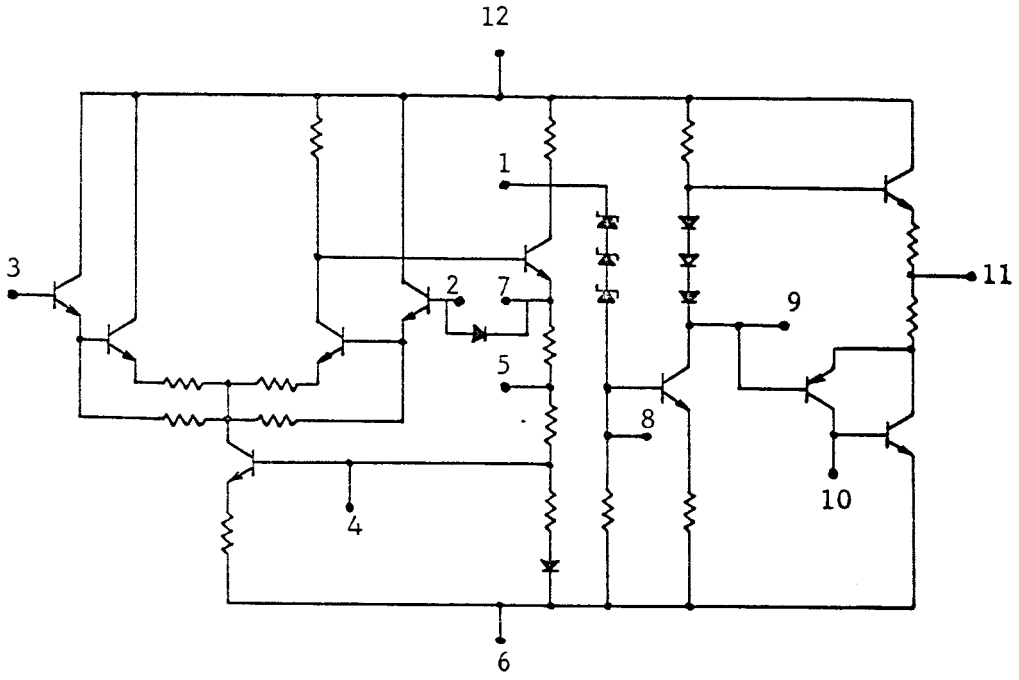
Conclusions and Recommendations

The preliminary nature of the work accomplished to date under this program does not warrant the drawing of any conclusions. It is, however, recommended that in future programs consideration be given to the purchase of state-of-the-art-type parts. It is felt that excessive delay in delivery of parts, and the delivery of subspecification parts for the present program have been time consuming and resulted in some inefficiencies. Our impression is that some of the problems may have been eliminated if the parts had been purchased.

APPENDIX I

TEST PLANS AND PROCEDURES

TEST PLAN FOR H-1



TEST CONDITIONS

1. Pin 12 - 12 volts
2. Pin 5 - ground
3. Pin 6 - -12 volts
4. Temperature - 25 C

TEST PARAMETERS

1. Circuit Gain and Dynamic Output
2. Bandwidth
3. Input Common Mode Rejection Ratio
4. Input Bias Current
5. Input Offset Voltage
6. Resistance
7. NPN Transistor D-C Beta
8. PNP Transistor D-C Beta

CHARACTERIZATION PLAN (AMPLIFIER)

CIRCUIT TYPE: H-1

BASIC CONDITIONS	NOTES
Pin 12 - 12 volts Pin 5 - ground Pin 6 - -12volts Temperature - 25 C	

PARAMETER	APP TEST	CONDITIONS
Circuit Gain	1	Apply a 5 vpp signal through a 20 K and 2.2 ohm divider into amplifier. Record peak-peak output signal. Open loop.
Dynamic Output	1	Increase input signal until output signal goes into saturation record both positive and negative saturation levels. Open loop.
Bandwidth	2	Frequency at which amplifier output drops off 3 db. Open loop.
Input Common Mode Rejection Ratio	3	Amplifier tied down to a gain of 100. Input signal was 1.0 kc and 1.0 volts rms.
Input Bias Current	4	Input to ground-open loop configuration
Input Offset Voltage	5	Set up open loop; adjust input voltage until zero volts appears at the output. The voltage applied to the input is the offset voltage.
Resistance	6	Resistance between Pins 6 and 8. Also resistance between Pins 1 and 12.

CIRCUIT TYPE: H-1

PARAMETER	APP. TEST	CONDITIONS
NPN Transistor D-C Beta	7	A 1 milliampere collector current is set and the base current is measured.
PNP Transistor D-C Beta	8	A 1 milliampere collect current is set and the base current is measured.

ENGINEER W. W. Schaffer DATE 10/25/65

REVISIONS:

CIRCUIT TYPE: H-1

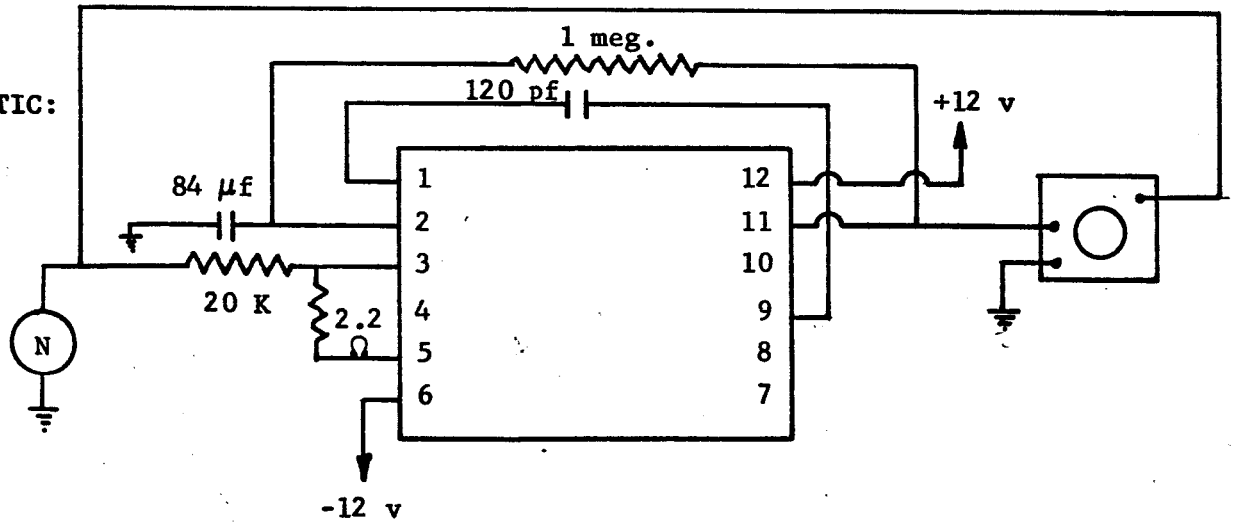
TEST NUMBER: 1

TEST TITLE: Circuit Gain and Dynamic Output

TEST CONDITIONS:

1. Connect circuit as shown on schematic
2. Use H.P. 200AB oscillator for the signal source.

SCHEMATIC:



TEST PROCEDURE:

1. Adjust the signal generator output to 5 v.p.p.
2. Record output signal peak-to-peak amplitude as V_O.
3. Increase signal generator output until both the positive and negative portions of the output signal are in saturation.
4. Record the positive and negative saturation levels with respect to ground as V_{SAT} and $-V_{SAT}$.

CIRCUIT TYPE: H-1

TEST NUMBER: 1

TEST PROCEDURE CONTINUED:

APPROXIMATE READINGS AND LIMITS EXPECTED

PARAMETERS	READINGS	LIMITS DURING TEST
V_O	11 volts	None
(±) V_{SAT}	9 volts	None

COMMENTS:

CIRCUIT TYPE: H-1

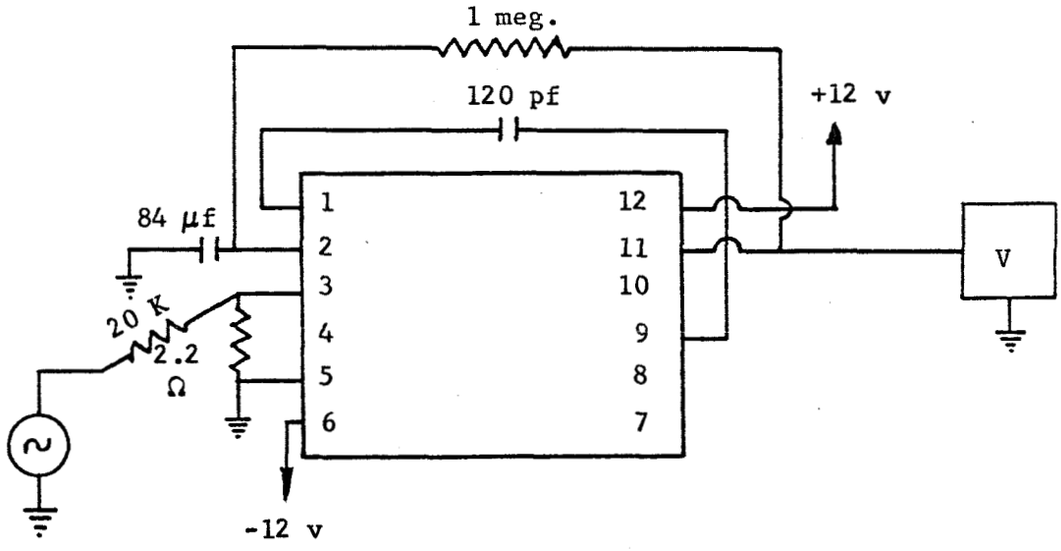
TEST NUMBER: 2

TEST TITLE: Bandwidth

TEST CONDITIONS:

1. Connect circuit as shown.
2. Use H.P. 200 AB for signal source.
3. Use Ballantine True RMS Voltmeter on the output.

SCHEMATIC:



TEST PROCEDURE:

1. Adjust the signal generator for +10 db at the amplifier output at 200 cps.
2. Increase signal generator frequency until the amplifier output decreases to +7 db.
3. Record signal generator frequency as B_w.

CIRCUIT TYPE: H-1

TEST NUMBER: 2

TEST PROCEDURE CONTINUED:

APPROXIMATE READINGS AND LIMITS EXPECTED

PARAMETERS	READINGS	LIMITS DURING TEST
B_w	~ 30 kc	1 kc - 40 kc

COMMENTS:

CIRCUIT TYPE: H-1

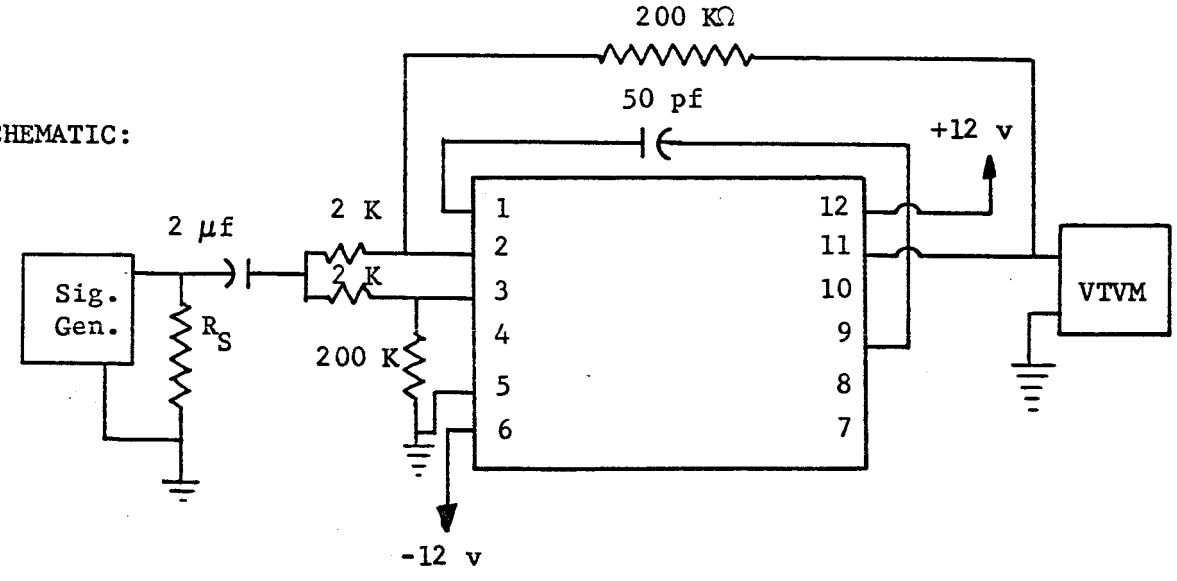
TEST NUMBER: 3

TEST TITLE: Input Common Mode Rejection Ratio

TEST CONDITIONS:

1. Apply +12 volts to Pin (12), -12 volts to Pin (6), and ground Pin (5).
2. Connect a 50 pf capacitor between Pin (1) and Pin (9).
3. Connect 200 KΩ resistors (matched to ±0.01%) between Pin (1).
4. Connect a sinusoidal signal generator to Pins (2) and (3) through a common 2 μf coupling capacitor and 2 KΩ resistors (matched to ±0.01%).
5. Connect a VTVM between Pin (11) and ground.

SCHEMATIC:



TEST PROCEDURE:

1. Set the signal generator frequency to 1.0 kc and the amplitude to 1.0 volts rms.
2. Measure and record the rms output voltage as V_{CM}.

CIRCUIT TYPE: H-1

TEST NUMBER: 3

TEST PROCEDURE CONTINUED:

APPROXIMATE READINGS AND LIMITS EXPECTED

PARAMETERS	READINGS	LIMITS DURING TEST
V_{CM}	10 mv	3 mv - 0.3 v

COMMENTS:

CIRCUIT TYPE: H-1

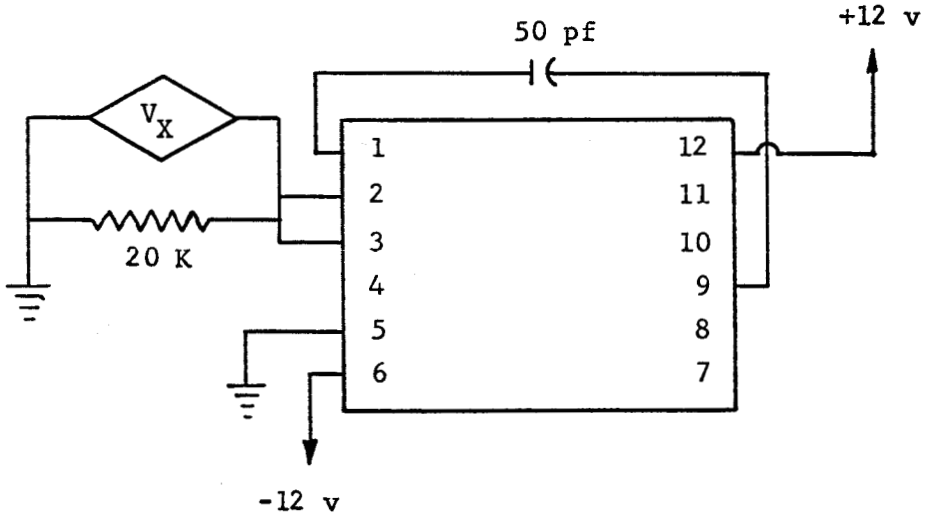
TEST NUMBER: 4

TEST TITLE: Input Bias Current

TEST CONDITIONS:

1. Apply +12 volts to Pin (12), -12 volts to Pin (6), and ground Pin (5).
2. Connect a 50 pf capacitor between Pin (1) and Pin (9).
3. Connect Pin (2) to Pin (3).
4. Connect a differential voltmeter and shunt 20 KΩ resistor between Pin (2) and ground.

SCHEMATIC:



TEST PROCEDURE:

1. Measure V_X and record as V_{in}.

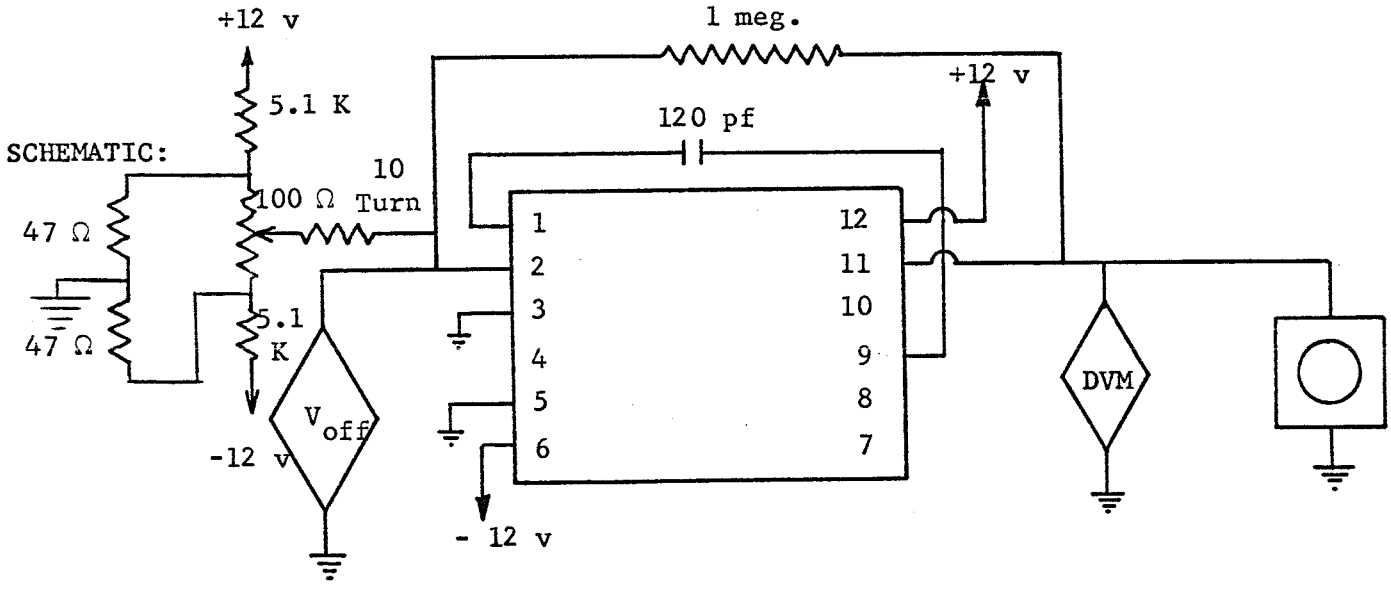
CIRCUIT TYPE: H-1

TEST NUMBER: 5

TEST TITLE: Input Offset Voltage

TEST CONDITIONS:

1. Connect circuit as shown.



TEST PROCEDURE:

1. Adjust the potentiometer for zero volts at Pin (11).
2. Measure the voltage at Pin (2) and record as V_{off}.

CIRCUIT TYPE: H-1

TEST NUMBER: 5

TEST PROCEDURE CONTINUED:

APPROXIMATE READINGS AND LIMITS EXPECTED

PARAMETERS	READINGS	LIMITS DURING TEST
V_{off}	5 mv	0 - 50 mv

COMMENTS:

CIRCUIT TYPE: H-1

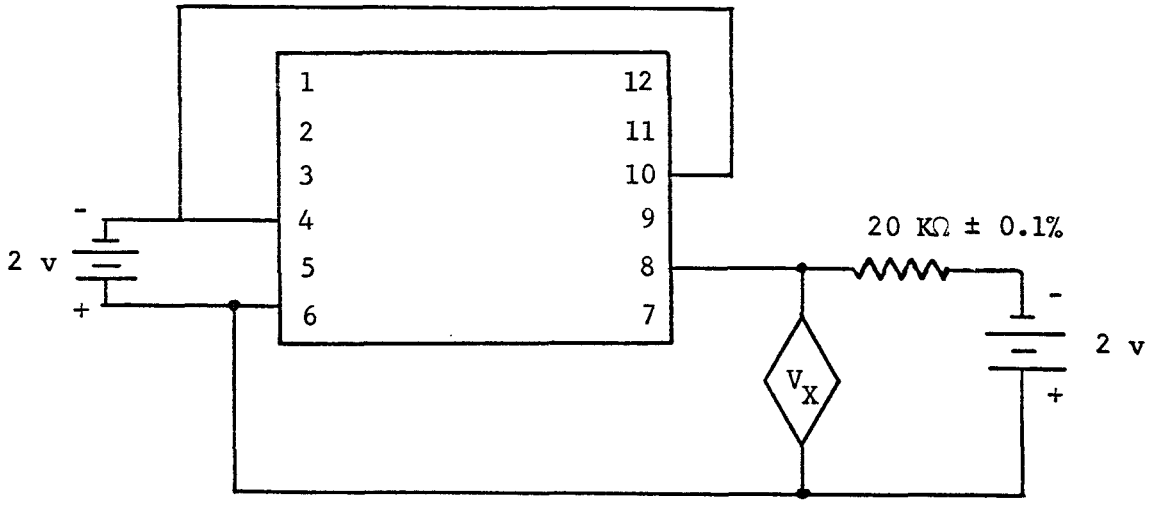
TEST NUMBER: 6

TEST TITLE: Resistance

TEST CONDITIONS:

1. Connect Pins (4) and (10) together.
2. Apply 2 volts between Pins (4) and (6). Negative terminal to Pin (4), positive terminal to Pin (6).
3. Connect the negative terminal of a second 2 volt supply to Pin (8) through a 30 K ±0.1% resistor. Connect the positive terminal to Pin (6).
4. Connect a differential voltmeter between Pins (8) and (6).

SCHEMATIC:



TEST PROCEDURE:

1. Measure and record V_X.
2. $R_{X_{(20\ K)}} = 20\ K \left(\frac{V_X}{2\ v - V_X} \right)$.
3. Remove all connections to circuit.
4. Connect positive side of resistance bridge to Pin 1 and negative side to Pin 12.
5. Record R_Y.

CIRCUIT TYPE: H-1

TEST NUMBER: 6

TEST PROCEDURE CONTINUED:

APPROXIMATE READINGS AND LIMITS EXPECTED

PARAMETERS	READINGS	LIMITS DURING TEST
V_X	1.0 volt	0.7 - 1.3 volt
R_Y	6.5 K-ohm	4 K - ∞

COMMENTS:

CIRCUIT TYPE: H-1

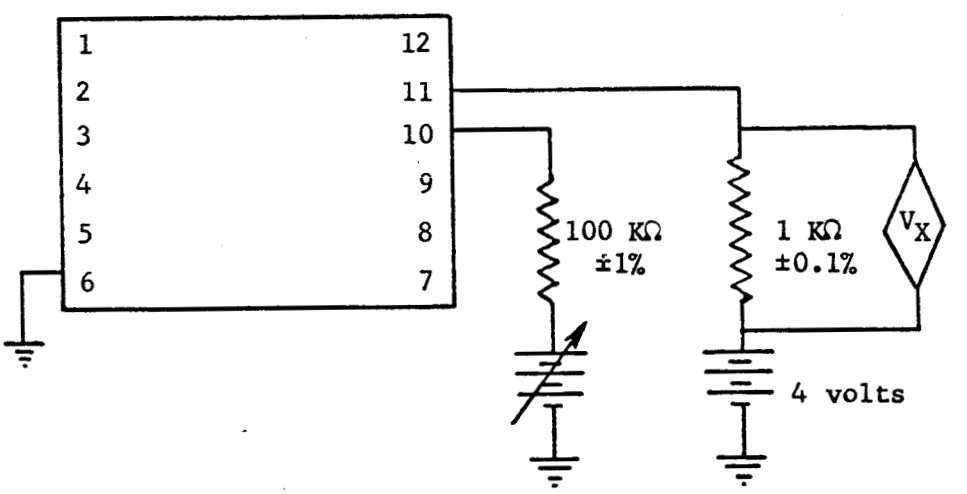
TEST NUMBER: 7

TEST TITLE: NPN Transistor D-C Beta

TEST CONDITIONS:

1. Ground Pin 6.
2. Connect the negative side of a power supply to ground and the positive side through a 100 KΩ ± 1 per cent resistor to Pin 10. Power supply set to 0 volt.
3. Connect the negative side of a 4-volt power supply to ground and the positive side through a 1 KΩ ± 0.1 per cent resistor to Pin 11.
4. Connect differential voltmeter across 1 K-ohm resistor.

SCHEMATIC:



TEST PROCEDURE:

1. Adjust V_1 until V_X indicates 1.0 volts.
2. Remove the differential voltmeter and apply across the 100 KΩ resistor.
3. Measure and record the reading of the differential voltmeter as V_{NPN}.
4. $\beta = \frac{V_X}{V_{NPN}} \quad \frac{100\ K}{1\ K} = \frac{1}{V_{NPN}} \times 100$.

CIRCUIT TYPE: H-1

TEST NUMBER: 7

TEST PROCEDURE CONTINUED:

APPROXIMATE READINGS AND LIMITS EXPECTED

PARAMETERS	READINGS	LIMITS DURING TEST
V_{NPN}	0.5	0 - 20 volts

COMMENTS:

The 240-ohm collector resistor will possibly introduce some error due to its change as a result of radiation. However, from past experience the change in resistance value should be so small as to be within the instrumentation error.

CIRCUIT TYPE: H-1

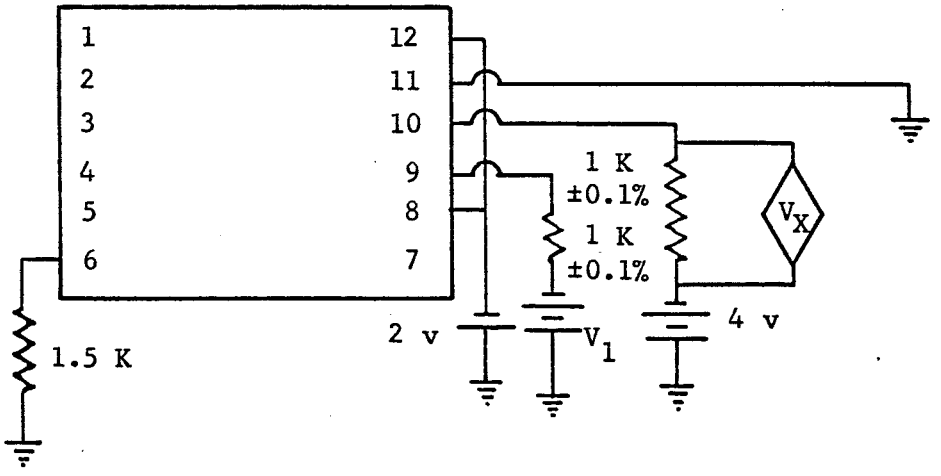
TEST NUMBER: 8

TEST TITLE: PNP Transistor D-C Beta

TEST CONDITIONS:

1. Ground Pin 11.
2. Connect the positive side of a 4 power ±0.001 volt supply to ground and the negative side through a 1 K-ohm ±0.1 per cent resistor to Pin 10.
3. Connect the positive side of a power supply to ground and the negative side through a 1 K-ohm ±0.1 per cent resistor to Pin 9. Set 0 volt on this power supply.
4. Connect Pins 8 and 12 together.
5. Connect a 1.8 K-ohm resistor to Pin 6.
6. Connect a -2 ±0.001 volts to Pin 8 (and 12).
7. Connect a differential voltmeter across the 1 K resistor connected to Pin 10.

SCHEMATIC:



TEST PROCEDURE:

1. Adjust V_1 until V_X indicates 1.0 volt.
2. Remove the differential voltmeter and connect between Pin 9 and negative terminal of V_1.
3. Record the reading of the differential voltmeter as V_{PNP}.
4. $\beta = \frac{V_X}{V_{PNP}} = \frac{1 \text{ volt}}{V_{PNP}}$.

CIRCUIT TYPE: H-1

TEST NUMBER: 8

TEST PROCEDURE CONTINUED:

APPROXIMATE READINGS AND LIMITS EXPECTED

PARAMETERS	READINGS	LIMITS DURING TEST
V_{PNP}	0.5 v	0.01 - 2 volts

COMMENTS: